A Literature Review on VLSI Implementation of Analog to Digital Converters

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Abstract. The signal processing is advancing day by day as its needs and in wireline/wireless communication technology from 2G to 4G cellular communication technology with CMOS scaling process. In this context the high-performance ADCs, analog to digital converters have snatched the attention in the field of digital signal processing. The primary emphasis is on low power approaches to circuits, algorithms and architectures that apply to wireless systems. Different techniques are used for reducing power consumption by using low power supply, reduced threshold voltage, scaling of transistors, etc. In this paper, we have discussed the different types and different techniques used for analog to digital conversion of signals considering several parameters.

1 Introduction

In digital processing systems, analog to digital converter (ADC) is a basal unit playing an imperative role as digital processing overweighs the analog processing in most of the applications. ADC bridges the analog trend with digital reign. For high demands, the ADC speed and power consumption are being made major concerns. Successive approximate register (SAR) ADC is acknowledged in many ADC applications for its efficacy in power and high competence in speed [1,2].

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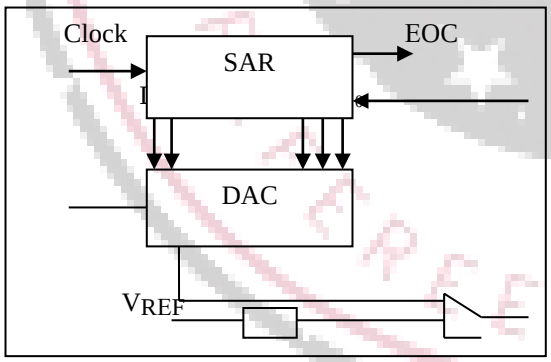

Fig. 1: Block Diagram of SAR ADC

The works mentioned in this paper employed different approaches to characterize ADC. In some approaches, quasi-static measurements like differential non linearity (DNL) and integral nonlinearity (INL) are measured and some approaches measure dynamic parameters like SNDR (signal to noise distortion ratio) and SFDR (spurious free dynamic range) using different tools

The ADC in successive approximate register type works basically as illustrated in the block diagram of fig.1. Analog to digital converters have many applications ranging from sensors, audio and DAS to video, radar and communication interfaces. In recent demands towards high-speed serial links where ADC is demanded of high speed and low power dissipation.

2 Review of Literature

The author M Sani and A Anasi Hamoui proposed an implementation of digital background calibration technique in 13-bit pipelined ADC and behavioral simulation of the same using SIMULINK, keeping σ = 0.25% of capacitor mismatches, the SNR value improvement is from 10 to 12.5 bits and SFDR of 95dB [3].

In 2008, Imran Ahmed presented a technique to calibrate 11- bit pipelined ADC for improving SNDR from 46.9 dB to 60 dB and SFDR from 48.9 dB to 70 dB using fabrication prototyped on 0.18 µm process and the calibration was done in the backend using the clock cycle of 10^4 [4]. In 2009, the authors proposed the concept of split calibration technique in 12- bits ADC to improve SFDR and SNDR using SIMULINK. In this article, the error in gain had been considered along with capacitor mismatch. It was showed by behavioural simulation the increase in SNDR and SFDR values from

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56.4 to 73.8 dB and the whole calibration process was performed in approximately 10^5 cycles [5].
The authors 'A Panigada and I Galton" have proposed two techniques for background calibration to counteract two problems of gain error and capacitor mismatch in pipelined ADC ie HDC (harmonics distortion correction) and DNC (DAC noise cancellation). Using HDC algorithm for gain error correction, implementation has achieved SNDR of 70 dB and SFDR of 85 dB in a 90nm CMOS process with power consumption of 130mW [6]. In 2011, Lee and Flynn worked with SAR ADC which achieved high energy efficiency with good resolution and high-speed operation resulting in low power using calibration free technique. The fabrication in 65 nm as well as in 90 nm CMOS was utilised to get the results of speed of 50MS/s and efficient number of bits of 10.4 b at Nyquist [7].
The author presented a 10 bits pipelined ADC in which switching opamps and digital calibration techniques are employed to achieve low power and low error gain using 65 nm CMOS technology for fabrication process. In this article, SNDR and SFDR values obtained are 55.4 dB and 67.2dB from a supply of 1V with low power consumption of 26.6mW and chip area of 0.36 mm^2 [8].
In one article of 2014, a prototyped time interleaved SAR ADC fabricated on 65 nm CMOS technology with high enhanced speed by Flash ADC among eight SAR ADCs was proposed. In this paper an approach of considering Flash ADC as reference for timing skew calibration technique to be used [9], clearly shown in the fig 2.

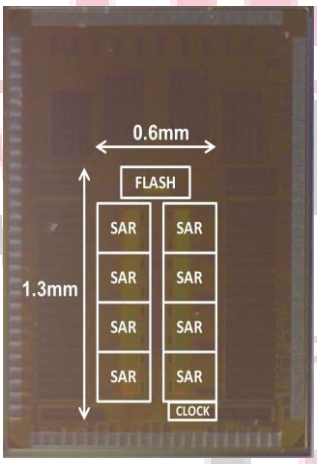

Fig. 2.: Die photograph of Time Interleaved ADC [9]

For high resolution SAR ADCs, a coarse reference ADC acceleration technique is employed in a new background calibration technique to improve convergence speed and ADCs linearity performance. The calibration is performed on the basis of IRD technique (internal redundancy dithering) [10].
The authors in 2015 employed a fully deterministic approach for digital calibration based on split 12-bit pipeline ADC at multistage level to find the circuit errors. The calibration was performed on a 200MS/s 40 nm CMOS for the modification in capacitor mismatch and amplifier gain. In this article, the behavioural simulation proved the area and power of the implemented 40nm 12-bit pipelined ADC 0.42mm^2 and 54 mW [11].

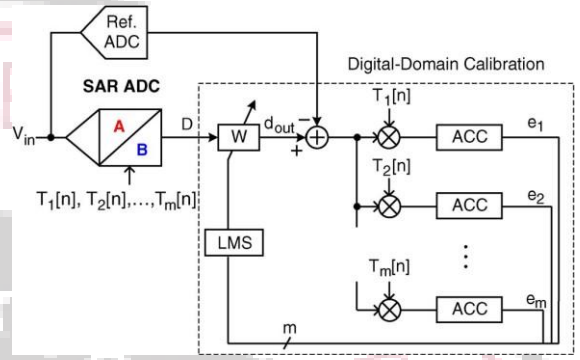

Fig. 3: IRD approach extended to treat m significant bits in SAR ADC. Also shown is a reference ADC that removes the input signal before bit-weight correlation takes place [10**].**

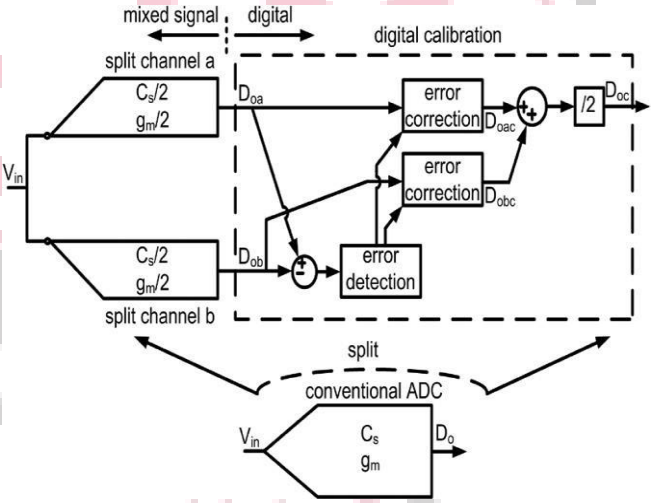

Fig 4: Split ADC background calibration concept [11]

Another work by A. Fahmy et al. on stochastic ADC was explained with its programmability and reconfigurability by dividing the whole design into 8 channels with a 10-bit control word. Using Verilog and digital design tools for synthesis fabricated on 130nm CMOS process, results were obtained in terms of SFDR and SNDR at 0.7V supply [12]. Another publication introduced and verified another technique of LMS (least algorithm mean squares) for background for calibration pipelined ADCs to correct conversion

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errors and DRDE (digitized residue distance estimation) algorithm [13]. The authors M.A. Montazerolghaem et. Al propose a digital background calibration technique with LMS algorithm to righteous the capacitor mismatch and error gains in which the conversion time is significantly reduced as compared to the same LMS techniques used in the other publication in the year 2014 by B. Zenali. The technique was simulated on 12-bit 100MS/s spilt pipelined ADC [14]. Another work attained shorter calibration times for split pipelined ADC and handled the non-orthogonality's of calibration loop. Using the calibration technique, the power dissipation in the residue amplifier was proved to be 60 % efficient and was estimated to be 192 mW with the SFDR and SNDR improvements [15].

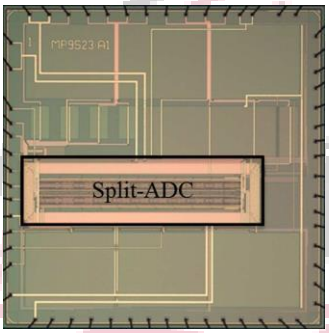

Fig 5: Chip micrograph of Split ADC [15]

In 2003, high speed 12-bits pipe-lined ADCs is presented for low power digital signal processing system in which the precision amplifiers are employed to cancel nonlinearities due to efficient simple power open-loop stages[16].In this, power reduction is done by the cancellation of non- linearities [16].

In this, the author has introduced a "split ADC" architecture running continuous digital background calibration technique in which the both ADCs used converts the same signal and after calibration, the outputs of both ADCs must be same and their difference produces null. In this, the algorithmic converter is realized as spilt ADC with 1000 conversions in self calibration. This consumes power of 1.5 milliwatts having die size of 1.2mm X 1.4 mm [17]. The authors L. Dorrer & F. Kuttner in 2005 explained that the low power is achieved by using three comparators in tracking ADC. The loop stability was increased and improved and also reduced the loop delay time. It is proven that the ADC is consuming power of 3 milliwatts with 1.5 – V supply at clock frequency of 104MHz. It is also proven that this design is consuming less power than that of the conventional start-of-the-art continuous time [18].
Also, A Zandieh et, al. presented a TI-ADC (time-interleaved Analog to digital converter) achieving more bandwidth and highest sampling rate with a 5-bit resolution using a comparator of low power and latch along with track and hold amplifiers [19].
In this, the author has presented a 12-bit pipelined ADC and proposed a digital background calibration technology to improve its performance in cancelling the errors like capacitor mismatch, errors in gain and nonlinearities produced, on 90nm CMOS technology [20].
One more related article proposing SAR assisted digital slope ADC, had brought the leads of both SAR and digital slope ADCs in a hybrid ADC. The prototype of hybrid ADCs was fabricated on 28nm CMOS technology resulting into very less power of 0.35mW and occupying less area of 66µm x 71µm [21], the micrograph chip of the same prototype is shown in fig 6.

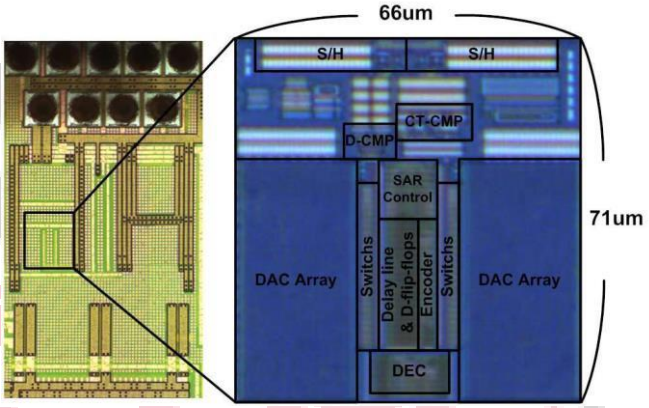

Fig 6: zoomed in view of ADC core [21]

A flash ADC is presented to improve chip area and performance speed with high resolution by employing multi segment encoder with MOS current mode logic (MCML) in the article [22]. In this article the novel structure maintains the simplicity of the encoder structure by using two segment encoders and a smaller number of multiplexers [22]. Another discussion on case study of pipelined ADC presented in the same year in which a vigorous calibration technique of multivalued ADC using the integral INL based calibration is obtained [23]. The paper [24] presented extended counting ADC without calibration to be applied in CMOS image sensors. In the same year a digitally assisted offset calibration technique is proposed by the authors for high speed open loop residual amplifier to achieve correct operation of 10-bit ADC and SNDR pf 22.5dB and SFDR of 11dB for 13-bit pipeline ADC [25].
In this, the power consumption was lowered by using a tracking ADC in which three comparators are exercised for wireless applications. The loop stability was increased and improved and also reduced the loop delay time. It is proven that; the ADC is consuming 3mW from a 1.5 – V supply when it is clocked at 104MHz. it is also proven that this design is consuming less power

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than that of the conventional start-of-the-art continuous time [26]. In this, simple power efficient open–loop stages are replaced in the place of precision amplifiers as precision amplifiers dominate the power dissipation in most high–speed pipe-lined ADCs. In this, power reduction is done by combining digital domain estimation and cancellation of non-linearities with simple power efficient open-loop stages. This can be used for efficient low power digital signal processing [27].

KB Vaibhav et al., presented a review article for high speed ADCs with comparison of different architectures with low power CMOS. The article details Flash ADCs, pipelined ADCs, SAR ADCs [28-30], subranging and two step ADCs, interpolating and folding ADCs to be suitable for the hybrid ADC design to perform high speed operations with the benefit in power values. The paper also talks about the hybrid ADC for applications demanding 1-GS/s with 6-bits resolution [31].

In 2019, the author Savitha et, al. has proposed a SAR-ADC with dual split 3-sections capacitive array DAC for IoT systems to obtain good accuracy for peer communication functioning like 14-bit SAR ADC [32] for low cost CMOS development. The authors T Hung et, al. proposed split ADC with digital background calibration for the improvement in the gain and INL errors in a pipelined ADC by employing 12-bit 400MS/s pipelined ADC [33]. The presented ADC in [34] used a slew rate boosting technique with Class C for saving power in the residual amplifiers of 12-bit architecture giving good slew rate performance by the author Mohd Naved et, al. SAR ADC are researched and described for different applications such as Biomedical applications, wireless sensors, receivers, etc. [35,36,37,39,40,42] for its high speed performance. Another type of ADC: Flash ADC [38,41,43] is also proposed for many applications such as high-speed instrumentation, radar, wireless sensor network, DSO, digital TVs and so on.

Some of the articles discussed and reviewed the various types of ADC and different calibration methods for timing skews in ADCs [44-51]. The SAR ADC [52-56] with pipelined ADC [57,58] combination is popularly in trend to get good performance from ADC along with CMOS scaling [59]. The reconfigurable ADC [60-64] are in research using pipelined and SAR ADCs to configure the resolution and sampling rate depending upon the requirements.

SAR ADC [68-72] is an analog circuit whose performance gets better with CMOS scaling process [73-75] and always employed for high speed, low power and high-resolution ADCs. The publication history of SAR ADC is noticeable from last two decades studying its performance enhancement [76-77].

In fig 7, the survey is plotted on the published articles based on SAR ADC till 2019 in VLIS and till 2020 in ISSCC, taken from the survey [78].

The prevailing research proves that the hybrid ADCs [65-67] architecture is more advantageous for enhancement in terms of speed and for low power operations [68]. The hybrid ADCs [79-82] have different combinations and blocks as per the applications demand. The designers can obtain better performances of ADC than in a monolithic chip with the help of Hybrid ADCs [83-90]. Employing Hybrid structured ADC [91-94], different parameters of ADC such as sampling rate, scaling, resolution, calibration free and so on can be improved.

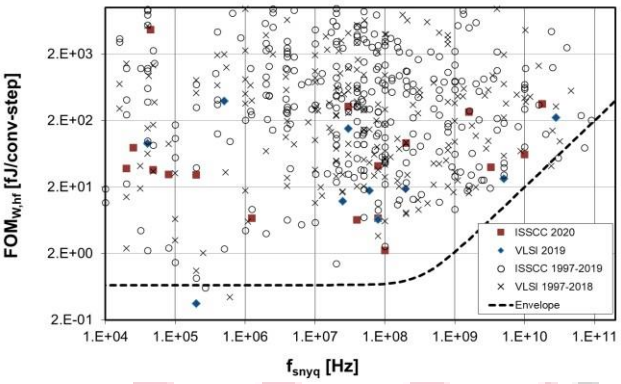

Fig 7: SAR ADC published till 2020 in ISSC and till 2019 in VLSI [78]

3 Results and Discussions

The Hybrid ADC comprising of pipelined SAR ADC with Digital Amplifiers concept was proposed, designed and implemented in 28nm CMOS achieving high speed of 320MS/s by observing on supply of both 0.7 V and 0.9 V, with SNDR of 60 dB [69]. The result FFT simulations of the pipelined SAR ADC were imported to MATLAB, for post simulation tests shown in figure 8. The proposal is to design a calibration free and CMOS scalable Hybrid ADC with digital amplifier instead of conventional OPAMPs.

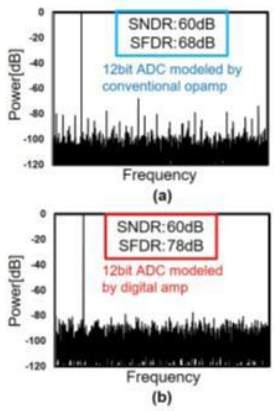

Fig. 8: FFT results of pipelined SAR ADC simulated on MATLAB with both conventional amplifiers and Digital Amplifiers [69].

4 Conclusion

The detailed survey is done on different types and various techniques of ADC and the summary of various features is presented using respective headings. Considering the merits and demerits of each techniques one should select the appropriate techniques for the end application. The analysis and trend prove the frequent employed of SAR ADC due its highly efficient with high speed performance and prominent scaling process. The features and limitations of various techniques are summarized and compared. The survey proposes to use Hybrid ADC using SAR pipelined ADC.

TABLE I. Comparison between various ADCs based on different parameters

Reference No.	Technology (µm)	Sampling rate (S/s)	Power consumption (W)	Supply voltage (V)	FOM (J/conversion step)	SNDR (dB)	Resolution
4	0.18	45 MS/s	-	1.8	-	70 dB	
6	0.09	-	130mW	-	-	70dB	-
12	0.13	100MS/s	1.5mW	0.7V	-	45dB	10 bits
18	0.13	-	3mW	1.5V	-	-	4 bits
17	0.25	1 MS/s	105mW	2.5V	-	-	16-bits
21	0.028	100MS/s	0.35mW	0.9V	2.6	64.43dB	-
35	0.13	1.6-GS/s	163m	1.2	4.08 p	29.7 dB	-
36	0.065	**1 GS/s**	**31.5 mW**	1.2	**20.9 fJ/step**	64.26 dB	12-bits
37	0.18	5 MS/s	8nW	1.8V	20fJ/conv.	-	-
38	0.065	900 MS/s	3.5mW	1V	32 fJ/conv.-step	49.5 dB	8-bits
39	-	1 MS/s	-	-	-	75.5 dB	14-bits
40	0.18	-	1 mW/element	1.8V	-	51.8	-
41	0.18	-	4.51mW	1.8V		30.1	
42	0.18	178.6KS/s	8 µW	1.8V	-	37dB	6-bits
52	0.045	-	330.5 µW	-	-	33.915dB	10 bits
53	0.13	**1 GS/s**	26mW	1.2V		49.7dB	6-bits
54	0.18µm	**10 GS/s**	1.5mW	1V	-	-	6-bits
70	0.04	**6.14MS/s**	6.43 µW	0.5V	7.1	44.3	-

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